

10nm CPI Study for Fine Pitch Flip Chip Attach Process and Substrate

by

Ming-Che Hsieh, Chi-Yuan Chen*, Ian Hsu*, Stanley Lin* and KeonTaek Kang**

Product and Technology Marketing / STATS ChipPAC Pte. Ltd.

10 Ang Mo Kio Street 65, Techpoint #04-08/09, Singapore 569059

*** Package Technology Division / MediaTek, Inc.**

**** Research and Development / STATS ChipPAC Pte. Ltd., Korea**

Originally published at 5thMicro/Nano-Electronics Packaging & Assembly, Design and

Manufacturing Forum,

Grenoble, France, May 17 – 18, 2017.

Copyright © 2017.

**By choosing to view this document, you agree to all provisions of the
copyright laws protecting it.**

10nm CPI Study for Fine Pitch Flip Chip Attach Process and Substrate

Ming-Che Hsieh, Chi-Yuan Chen*, Ian Hsu*, Stanley Lin* and KeonTaek Kang**

Product and Technology Marketing / STATS ChipPAC Pte. Ltd.

10 Ang Mo Kio Street 65, Techpoint #04-08/09, Singapore 569059

E-mail: mc.hsieh@statschippac.com

* Package Technology Division / MediaTek, Inc.

** Research and Development / STATS ChipPAC Pte. Ltd., Korea

Abstract

The rapid growth rate of advance technology developments in the semiconductor industry is driving the evolution in emerging markets to satisfy the increasing requirements of higher performance, higher bandwidth and lower power consumption as well as multiple functions in portable and mobile devices. Electronic devices have evolved from a simple communication device to a complicated and highly integrated system with multiple functions required. Moving forward with this trend, packaging semiconductor devices for mobile electronics is

is still the major issue to be addressed. As the substrate cost is always the significant factor in a flip chip package, flip chip assembly with a low cost substrate has become a hot topic in the industry. In the flip chip assembly process, substrate technology has been moving from traditional bond-on-capture (BOC) pad with cored substrate to bond-on-lead (BOL) with coreless substrate in recent years. Embedded trace substrate (ETS) has been widely adopted for low cost requirements. In addition, flip chip interconnect with copper (Cu) pillar BOL and enhanced processes (fcCuBE[®]) can help to deliver a high performance packaging solution with a cost effective mass reflow (MR) manufacturing process [6-7]. By using the above technologies, it has been proven that not only can it meet the packaging cost reduction, but it can also achieve a thin flip chip package profile.

Due to the fast growth in emerging markets for mobile applications, advanced Si node

also passed long term reliability tests such as pre-condition of moisture sensitivity level (MSL2aA and MSL3) as well as unbiased highly accelerated stress test (uHAST) of 96 hours and thermal cycling test condition B (TCB) of 1000 cycles without any defect observed. The package reliability results with Leg#2 and 3 assessments are illustrated in Figure 7 based on utilizing Through Scanning Acoustic Microscopy (T-SAM) inspection. The result shows that the illustrated robust flip chip attach processes examined in this

Figure 2: QTC results through C-SAM inspection in Leg#1.

Figure 3: SEM cross-sectional images in Leg#2 and 3 after QTC60x.

Since package warpage and coplanarity behavior are typically requested to meet Surface Mount Technology (SMT) processes without any issue, maximum warpage of $80\mu\text{m}$ at high temperature (260°C) and maximum coplanarity of $80\mu\text{m}$ in specific dimensions are always required in flip chip technology [5, 8]. Figure 4 illustrates the warpage behavior distribution at every temperature read points in this fcCSP, which clearly indicates that all three legs can meet the package warpage specification of less than $80\mu\text{m}$ at every temperature read point and the maximum warpage can be reduced to less than $60\mu\text{m}$. In addition, through the coplanarity assessment, it is found that all three legs can meet the requirement and with the use of PPG-A will have better coplanarity control, which is shown in Figure 5.

As the flip chip bump pitch become finer, solder bridge risk during the MR chip attach process is always the key issue to be overcome. In order to understand if there is any solder bridge phenomenon occurring during the flip chip assembly process, the confirmation build of 1000 units sample size (with dummy dies) with Leg#2 condition is estimated to evaluate the package assembly yield. Figure 6 illustrates the assembly yield result by using X-ray/External Visual Inspection (EVI), which indicates that no solder bridge was observed during the fcCSP assembly build. Moreover, this fcCSP with 10nm ELK backend process daisy-chain die

Figure 7: Long term package reliability result in

reflow profile (OPT) is established. Table 5 shows the corresponding QTC result in a 10nm fcCSP with 200µm die thickness. As shown on Table 5, it is found that with the optimized chip attach reflow profile (one-time ref

